Figure 1

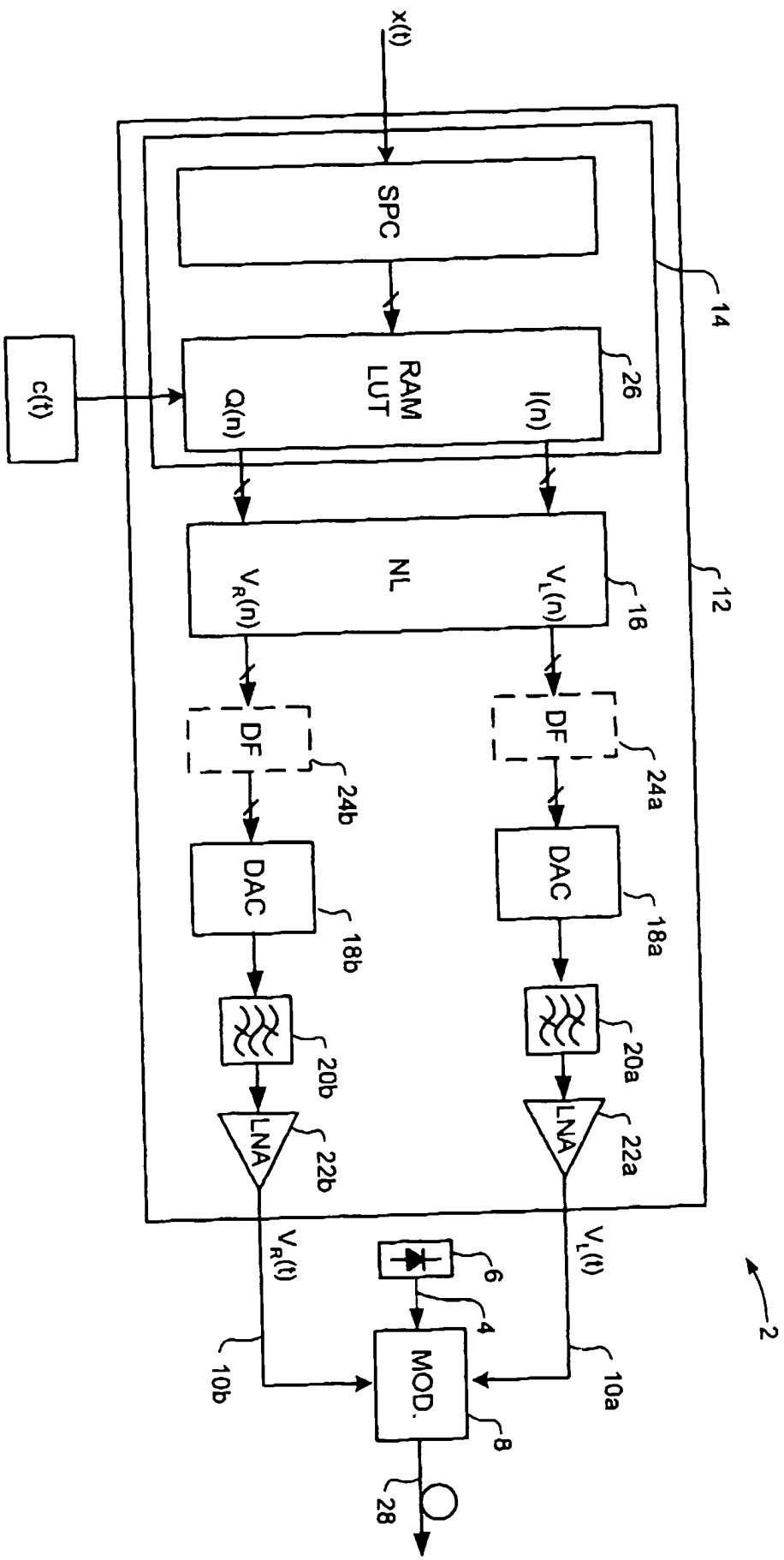
x(t)
SPC
14
c(t)
RAM
LUT
26
Q(n)
I(n)
NL
$V_R(n)$
$V_L(n)$
16
12
DF
24b
DF
24a
DAC
18b
DAC
18a
20b
20a
LNA
22b
LNA
22a
$V_R(t)$
$V_L(t)$
6
4
MOD.
8
10b
10a
28
2

Figure 2

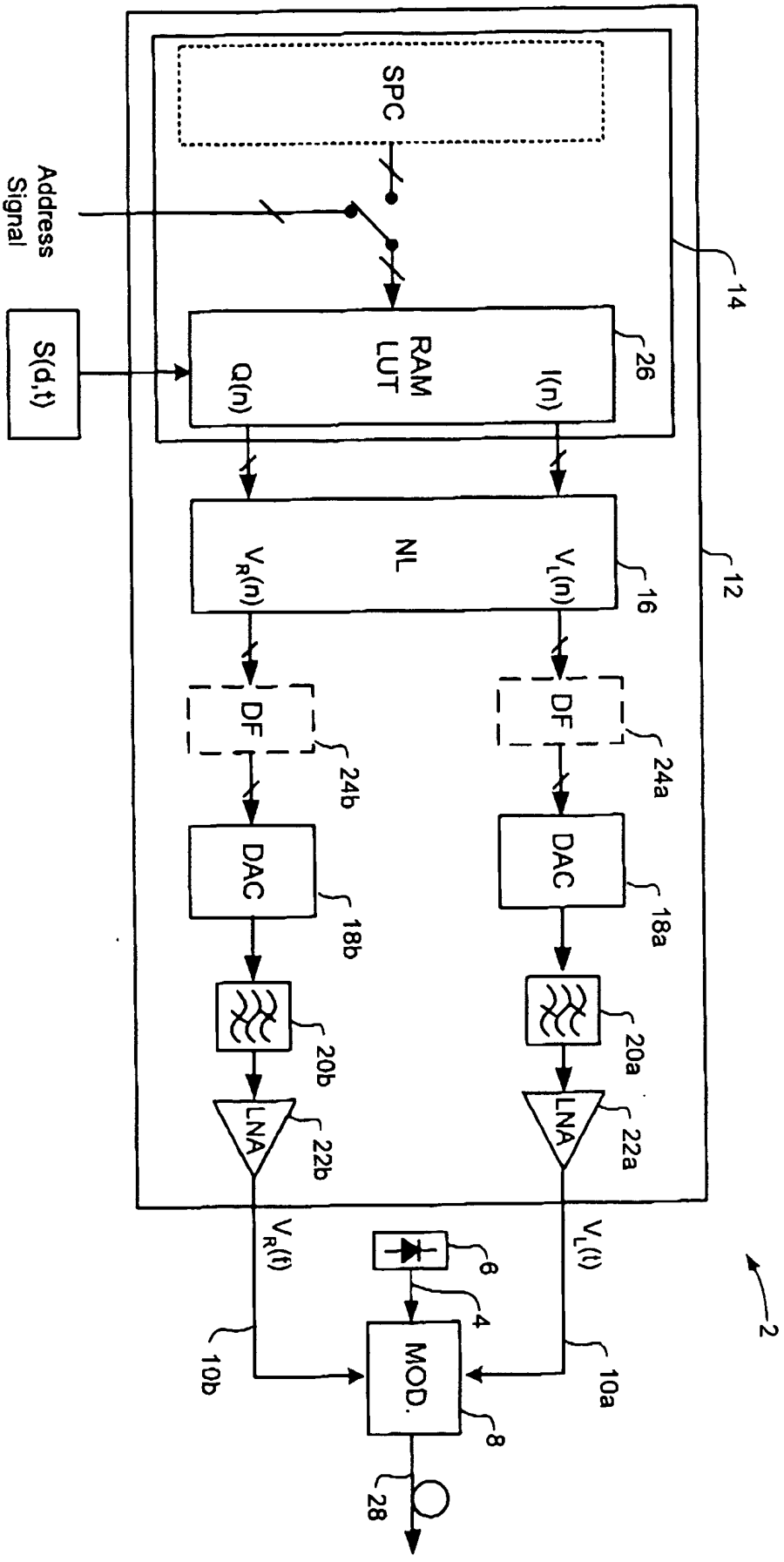
SPC
Address Signal
S(d,t)
RAM LUT
Q(n)
I(n)
26
14
NL
$V_R(n)$
$V_L(n)$
16
12
DF
24b
24a
DAC
18b
18a
20b
20a
LNA
22b
22a
$V_R(t)$
$V_L(t)$
6
4
MOD.
8
10b
10a
28
2

Figure 3a

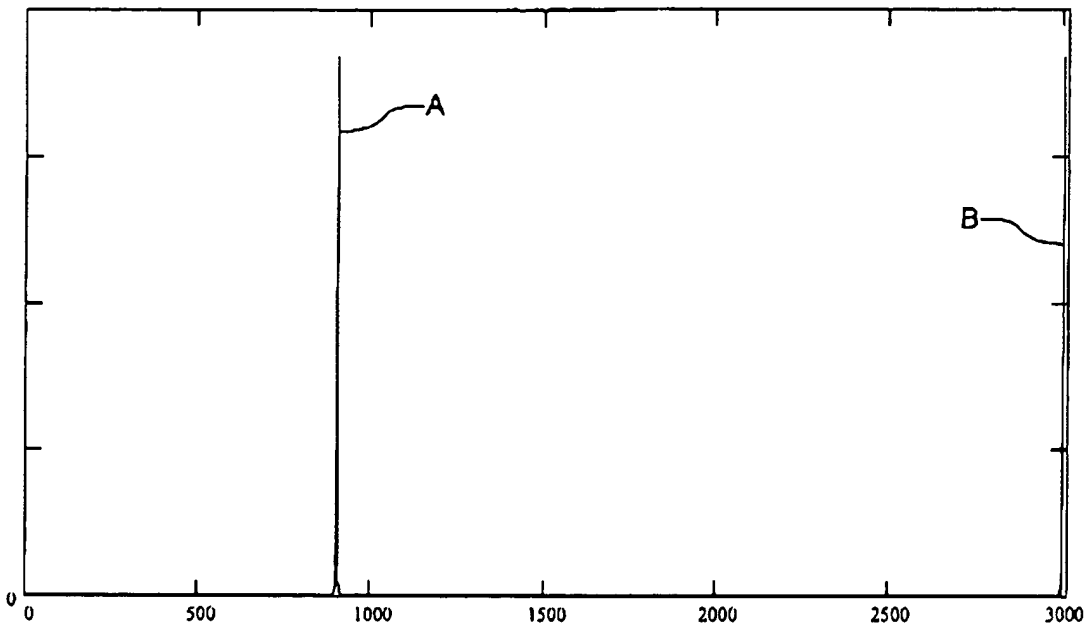

Figure 3b

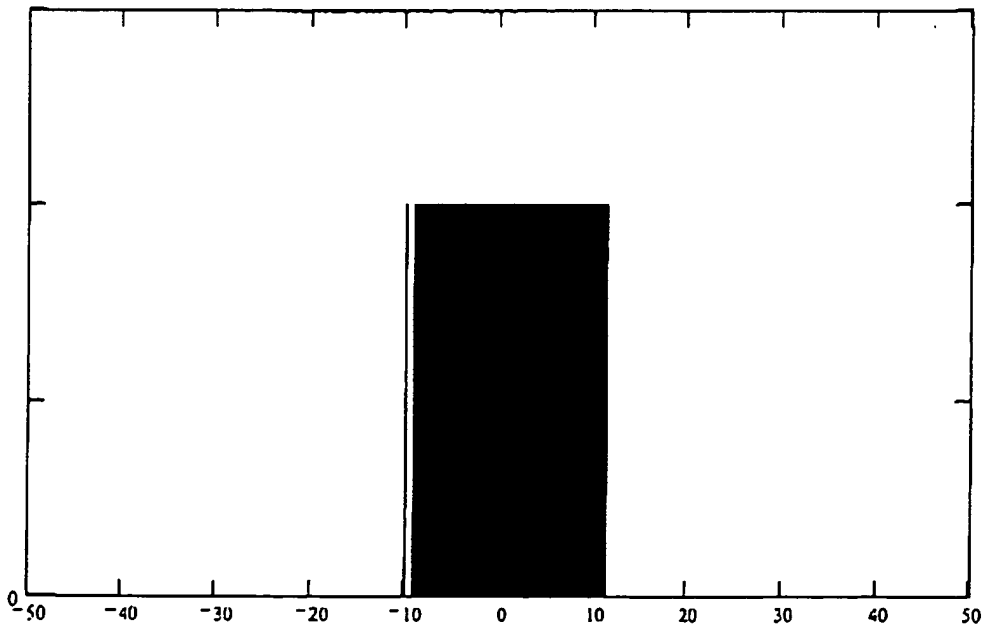

Figure 3c

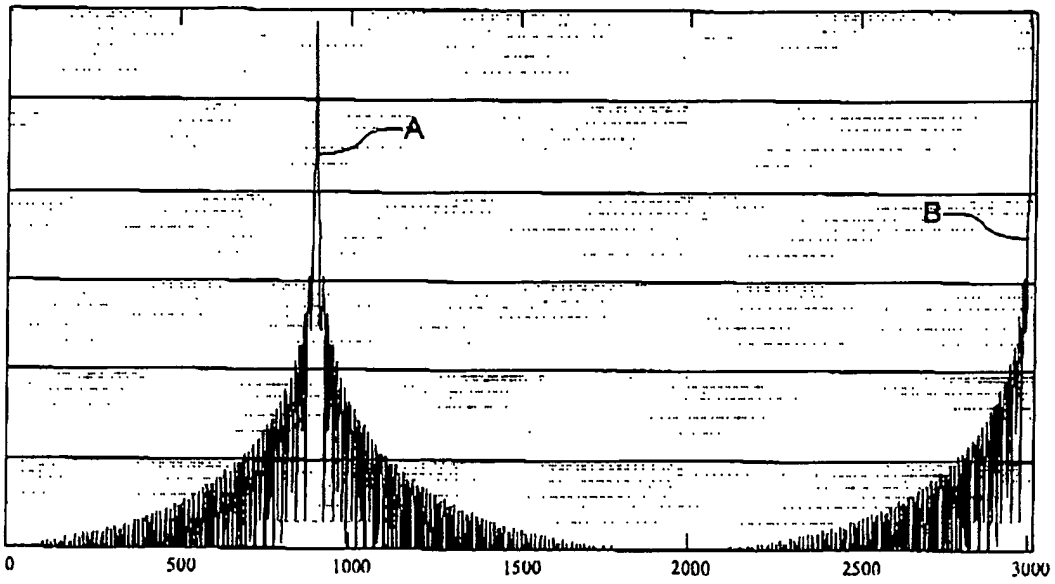

Figure 3d

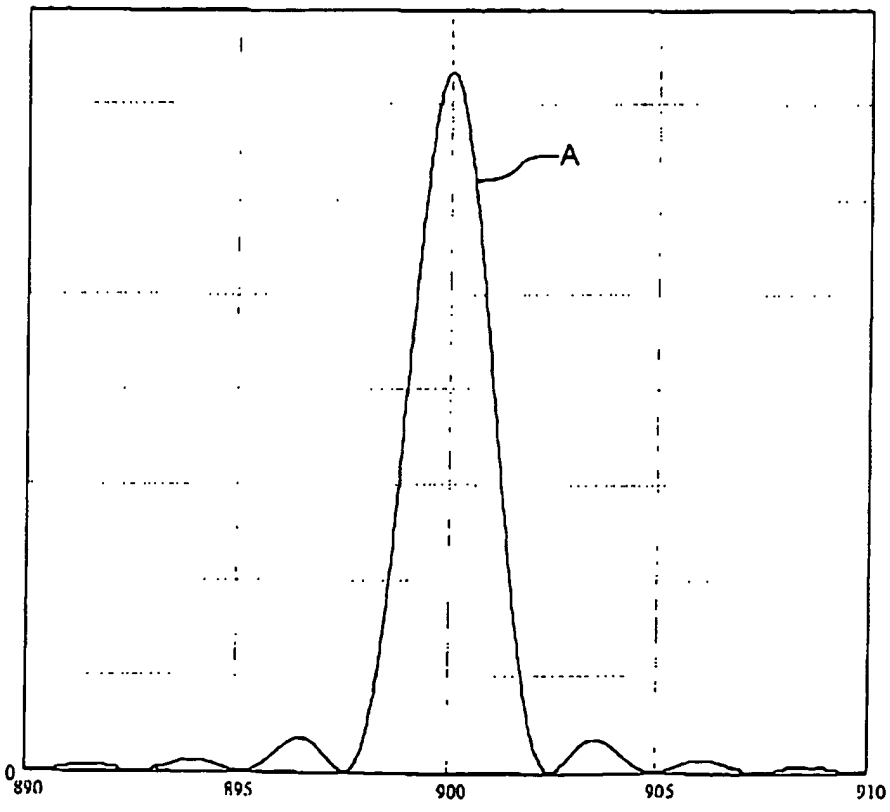

Figure 3e

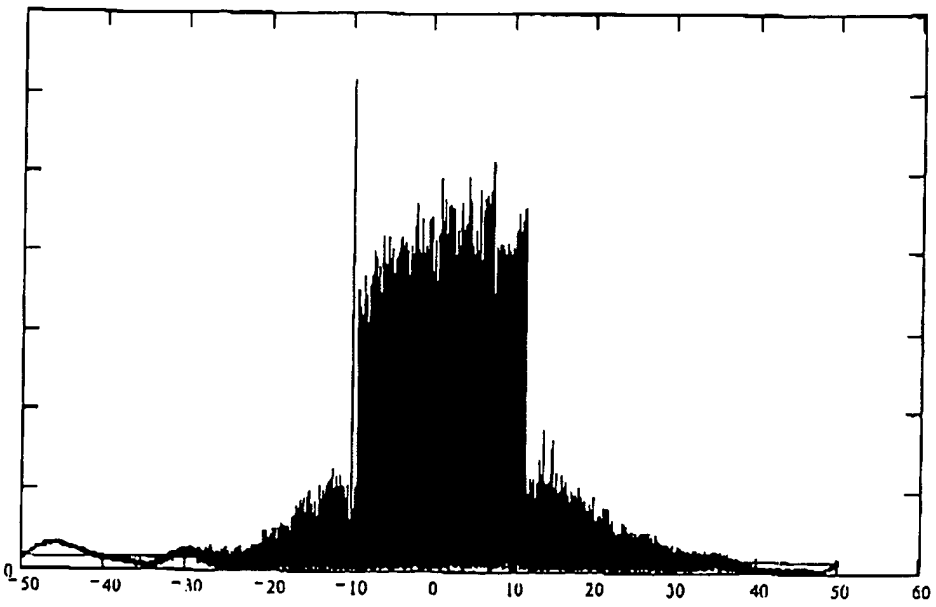

Figure 3f

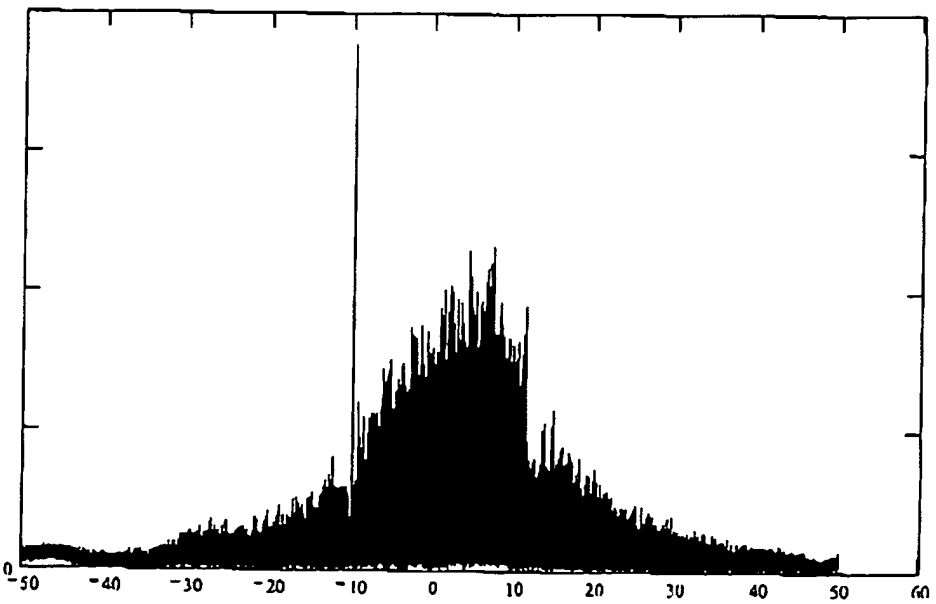

Figure 3g

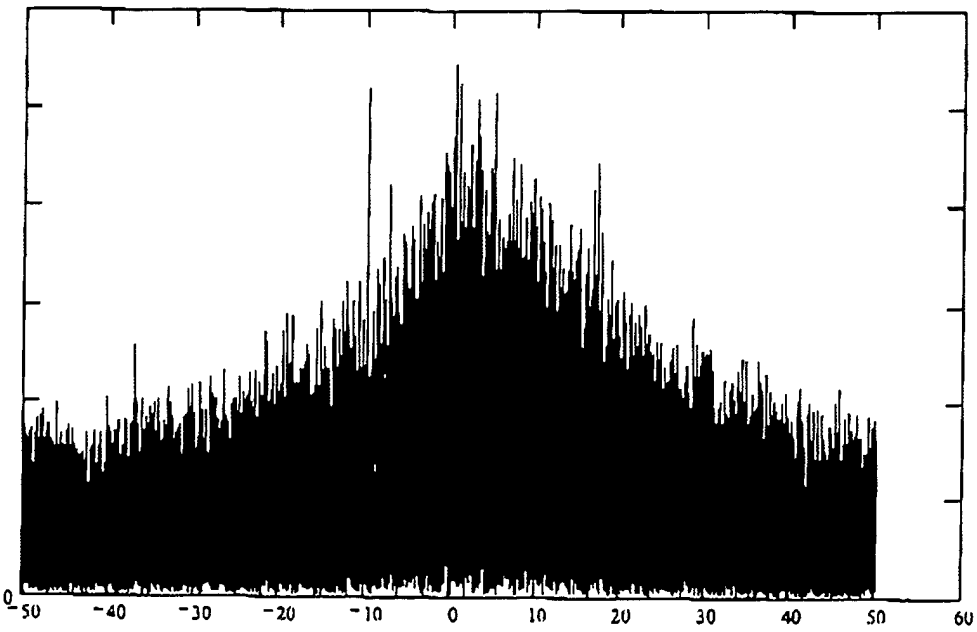

Figure 3h

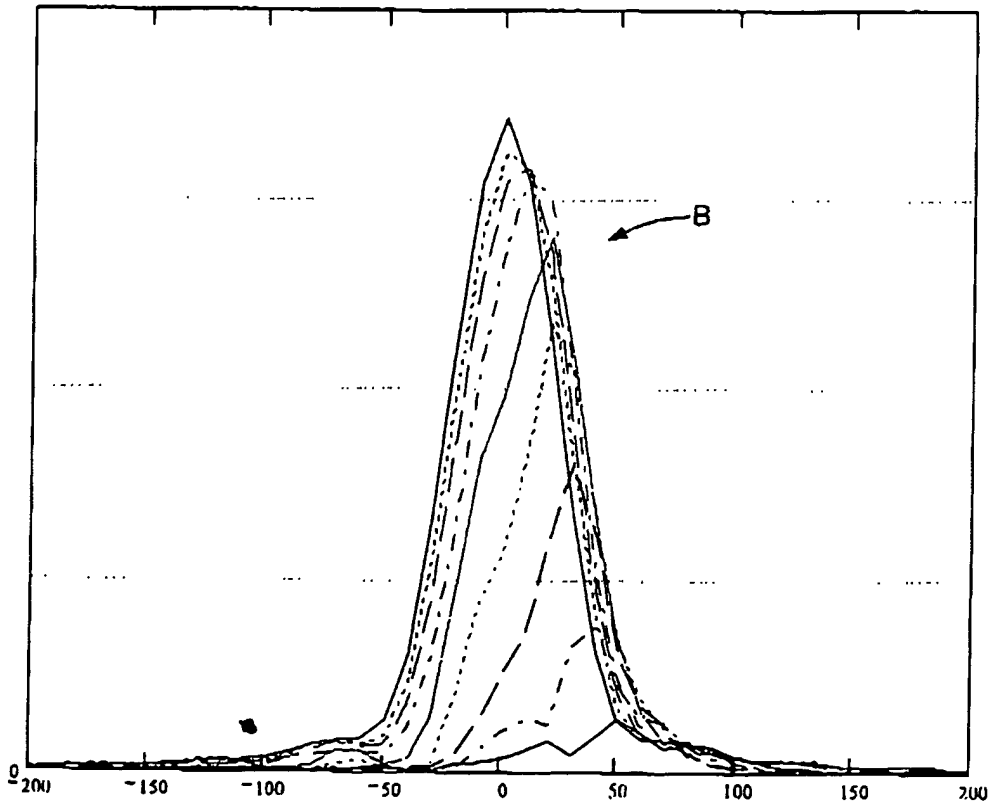

Figure 4a

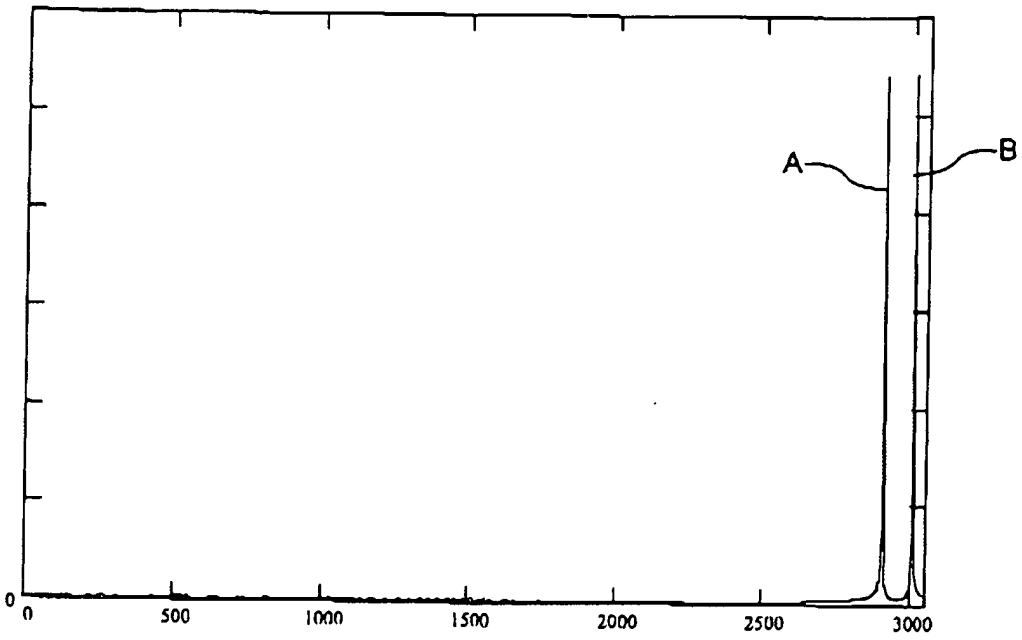

Figure 4b

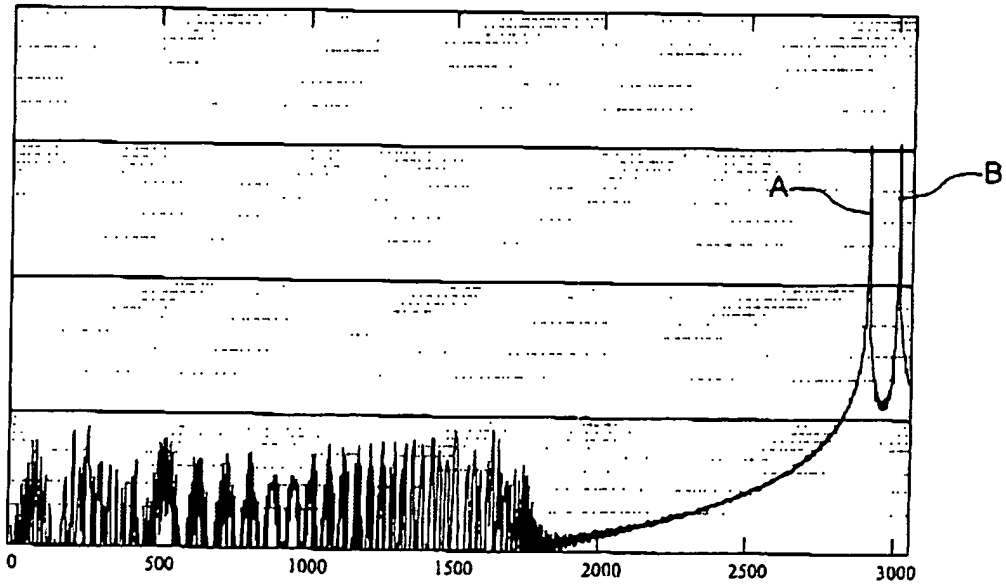
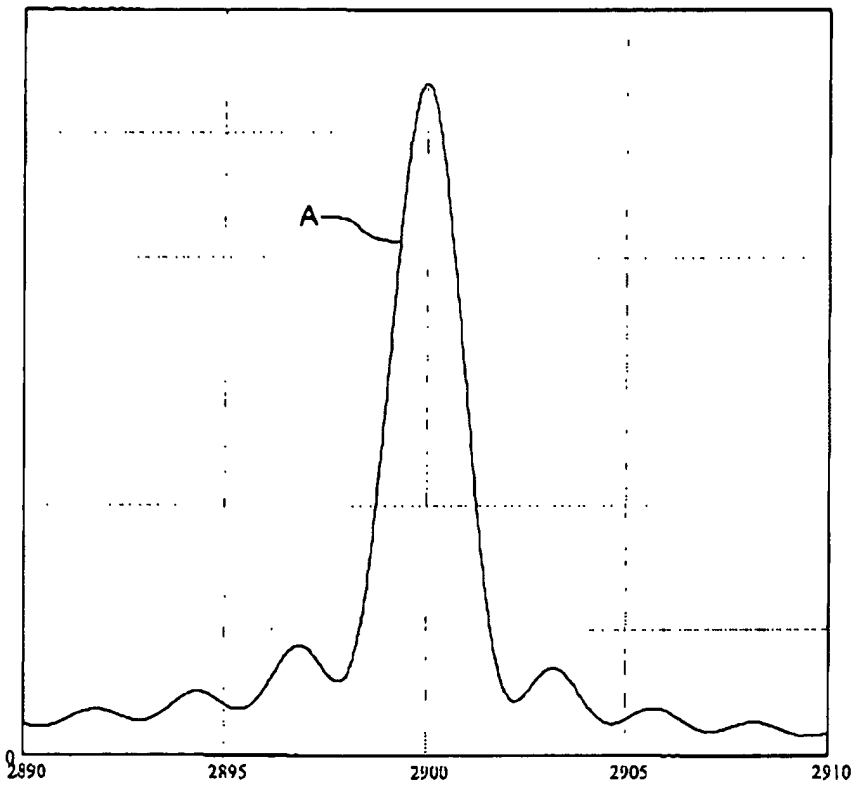
Figure 4c